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EV550715587

P.O. SB/21 (09-04)

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FORM**

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Total Number of Pages in This Submission

12

Application Number

09/848,846

Filing Date

May 3, 2001

First Named Inventor

Luân C. Tran

Art Unit

2813

Examiner Name

Laura M. Schillinger

Attorney Docket Number

MI22-1689

**ENCLOSURES (Check all that apply)**

Fee Transmittal Form



Fee Attached



Amendment/Reply



After Final



Affidavits/declaration(s)



Extension of Time Request



Express Abandonment Request



Information Disclosure Statement



Certified Copy of Priority Document(s)

Reply to Missing Parts/  
Incomplete ApplicationReply to Missing Parts  
under 37 CFR 1.52 or 1.53

Drawing(s)



Licensing-related Papers



Petition

Petition to Convert to a  
Provisional Application

Power of Attorney, Revocation



Change of Correspondence Address



Terminal Disclaimer



Request for Refund



CD, Number of CD(s) \_\_\_\_\_

☐ Landscape Table on CD

After Allowance Communication to TC

Appeal Communication to Board  
of Appeals and InterferencesAppeal Communication to TC  
(Appeal Notice, Brief, Reply Brief)

Proprietary Information



Status Letter

Other Enclosure(s) (please identify  
below):

Check; PTO Return Receipt Postcard

Remarks

No extension fees are believed to be due.

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm Name

Wells St. John P.S. (Customer No. 021567)

Signature

Printed name

Deepak Malhotra

Date

June 23, 2005

Reg. No.

33,560

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EV550715585 PTO/SB/17 (12-04v2)  
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Effective on 12/08/2004. Fees subject to the Consolidated Appropriations Act, 2005 (H.R. 4818).		<b>Complete if Known</b>	
<b>FEE TRANSMITTAL</b> <b>For FY 2005</b>		Application Number	09/848,846
		Filing Date	May 3, 2001
		First Named Inventor	Luan C. Tran
		Examiner Name	Laura M. Schillinger
		Art Unit	2813
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27		Attorney Docket No.	MI22-1689
TOTAL AMOUNT OF PAYMENT (\$)		500.00	

**METHOD OF PAYMENT** (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): \_\_\_\_\_

☒ Deposit Account Deposit Account Number: \_\_\_\_\_ Deposit Account Name: \_\_\_\_\_

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**FEE CALCULATION**

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

**2. EXCESS CLAIM FEES**

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

**Total Claims** \_\_\_\_\_ **Extra Claims** \_\_\_\_\_ **Fee (\$)** \_\_\_\_\_ **Fee Paid (\$)** \_\_\_\_\_

\_\_\_\_\_ - 20 or HP = \_\_\_\_\_ x \_\_\_\_\_ = \_\_\_\_\_

HP = highest number of total claims paid for, if greater than 20.

**Indep. Claims** \_\_\_\_\_ **Extra Claims** \_\_\_\_\_ **Fee (\$)** \_\_\_\_\_ **Fee Paid (\$)** \_\_\_\_\_

\_\_\_\_\_ - 3 or HP = \_\_\_\_\_ x \_\_\_\_\_ = \_\_\_\_\_

HP = highest number of independent claims paid for, if greater than 3.

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
_____	_____	_____	_____	_____
_____ - 100 = _____ / 50 = _____ (round up to a whole number) x _____ = _____				

**4. OTHER FEE(S)**

Non-English Specification, \$130 fee (no small entity discount) **Fees Paid (\$)** \_\_\_\_\_

Other (e.g., late filing surcharge): Appeal Brief Filing Fee **Fees Paid (\$)** 500.00

<b>SUBMITTED BY</b>		
Signature		Registration No. (Attorney/Agent) 33,560
Name (Print/Type)	Deepak Malhotra	Telephone 609-624-4276
		Date June 23, 2005

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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EV550715587

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BOARD OF PATENT APPEALS AND INTERFERENCES

Application Serial No. .... 09/848,846  
Confirmation No..... 1789  
Filing Date..... May 3, 2001  
Inventor..... Luan C. Tran  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2813  
Examiner ..... Laura M. Schillinger  
Attorney's Docket No..... MI22-1689  
Customer No. .... 021567  
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

**APPEAL BRIEF**

To: Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

From: Deepak Malhotra (Tel. 509-624-4276; Fax 509-838-3424)  
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601 W. First Avenue, Suite 1300  
Spokane, WA 99201-3828

Appellant is appealing from the Final Rejection of claims 11-12, and 14 in an Office Action dated March 23, 2005. A check for required fee in the amount of \$500.00 specified under 37 C.F.R. § 41.20(b)(2) for filing this Appeal Brief is enclosed.

**Real Party In Interest**

The real party in interest is Micron Technology, Inc.

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500.00 DP

### Related Appeals and Interferences

There are no other appeals which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

### Status of Claims

Claims 11-12, and 14 are pending. All of claims 11-12, and 14 stand finally rejected. The claims appealed are claims 11-12, and 14.

### Status of Amendments

No amendments were filed subsequent to the final rejection.

### Summary of Claimed Subject Matter

Some aspects of the invention, defined by claim 11, provide a semiconductor processing method. The method comprises a masking step providing a common mask (p.10,ln.1-5; Fig.6). The method further comprises an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages (p.10,ln.1-16; Fig.6). The common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices (p.7,ln.13-p.8,ln.5; Figs.3,6).

Aspects of the invention, defined by claim 12, provide a semiconductor processing method. The method comprises a masking step

providing a common mask (p.10,ln.5; Fig.6). The method further comprises an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages (p.10,ln.1-16; Fig.6). The common masking step comprises masking only portions of some of the devices which receive the halo implant (p.7,ln.13-17; Figs.3,6). The devices which receive the halo implant comprise NMOS field effect transistors (p.10,ln.1-10; Fig.6). The portions comprise portions of peripheral circuitry devices. (p.7,ln.13-p.8,ln.5, p.10,ln.1-6; Figs.3,6).

Aspects of the invention, defined by claim 14, provides a semiconductor processing method. The method comprises a masking step providing a common mask (p.10,ln.1-5; Fig.6). The method further comprises an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages (p.10,ln.1-16; Fig. 6). The common masking step comprises masking only portions of some of the devices which receive the halo implant (p.7,ln.13-p.8,ln.5; Figs.3,6). The devices which receive the halo implant comprise PMOS field effect transistors (p.6,ln.14-p.7,ln.6; Figs. 2,3). The portions comprise portions of peripheral circuitry devices (p.7,ln.13-p.8,ln.5; Figs.3,6).

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### Grounds of Rejection to be Reviewed on Appeal

Whether or not claims 11-12 and 14 are patentable under 35 U.S.C. §103 over U.S. Patent No. 5,252,504 to Lowrey et al.

### Argument

Claims 11-12 and 14 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,252,504 to Lowrey et al.

Claim 11, for example, recites an implant step carried out through a common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

The Examiner admits that Lowrey fails to teach three different transistors having three different threshold voltages. The Examiner states that the courts have held that mere duplication of parts has no patentable significance unless a new or unexpected result is produced, and is relying on *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

The Court in *Harza* stated that the only difference between the reference's structure for sealing concrete and that of *Harza's* claim 1 was that the reference's structure had only a single rib (i.e., arm) on each side of a web, whereas the claim required a plurality of such ribs. See *Harza*, 274 F.2d at 671, 124 USPQ at 380. The Court stated that "[i]t is well settled that the mere duplication of parts has no patentable significance unless a new

and unexpected result is produced, and we are of the opinion that such is not the case here.”

The Examiner did not compare the facts in *Harza* with those in the present case and did not explain why, based upon this comparison, the legal conclusion in the present case should be the same as that in *Harza*. Instead, the Examiner relies upon *Harza* as establishing a *per se* rule that duplication of parts is obvious. As stated by the Federal Circuit in the more recent case of *In re Ochiai*, 71 F.3d 1565, 1572, 37 USPQ2d 1127, 1133 (Fed. Cir. 1995), “reliance on *per se* rules of obviousness is legally incorrect and must cease.”

For a *prima facie* case of obviousness to be established, the teachings from the prior art itself must appear to have suggested the claimed subject matter to one of ordinary skill in the art. See *In re Rinehart*, 531 F.2d 1048, 1051, 189, USPQ 143, 147 (CCPA1976).

The mere fact that the prior art could be modified as proposed by the Examiner is not sufficient to establish a *prima facie* case of obviousness. See *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). The Examiner must explain why the prior art would have suggested to one of ordinary skill in the art the desirability of the modification. See *In re Fritch*, 972 F.2d at 1266, 23 USPQ2d at 1783-84. The Examiner has not provided any reason why one of ordinary skill in the art would have included three different transistors having three different threshold voltages.

The Examiner has not explained why the Lowrey reference itself would have fairly suggested, to one of ordinary skill in the art, the desirability

of three different transistors with three different threshold voltages rather than Lowrey's two transistors.

For the above reasons, the Examiner has not established a *prima facie* case of obviousness and the rejections should be reversed.


Additionally, insufficient evidence has been provided as to why one of ordinary skill in the art would have been motivated to select the Lowrey reference and modify it in the manner suggested by the Examiner. Attention is directed to *In re Sang-Su Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002).

The factual inquiry whether to combine references must be thorough and searching. It must be based on objective evidence of record. No actual evidence has been provided why one of ordinary skill in the art would have included three different transistors having three different threshold voltages.

In view of the foregoing, reversal of the final rejection of claims 11-12 and 14 is requested.

Respectfully submitted,

Date: June 23, 2005

  
\_\_\_\_\_  
Deepak Malhotra  
Reg. No. 33,560



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Serial No. ....09/848,846  
Confirmation No..... 1789  
Filing Date..... May 3, 2001  
Inventor.....Luan C. Tran  
Assignee .....Micron Technology, Inc.  
Group Art Unit .....2813  
Examiner ..... Laura M. Schillinger  
Attorney's Docket No. ....MI22-1689  
Customer No. ....021567  
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

**Claims Appendix**

The claims involved in the appeal are as follows:

Claim 11: A semiconductor processing method comprising:  
a masking step providing a common mask; and  
an implant step carried out through the common mask, comprising  
conducting a halo implant of devices formed over a substrate comprising  
memory circuitry and peripheral circuitry sufficient to impart to at least three  
of the devices three different respective threshold voltages, wherein the  
common masking step comprises masking only portions of some of the  
devices which receive the halo implant, said portions comprising portions of  
peripheral circuitry devices.

Claim 12: A semiconductor processing method comprising:  
a masking step providing a common mask; and  
an implant step carried out through the common mask, comprising  
conducting a halo implant of devices formed over a substrate comprising  
memory circuitry and peripheral circuitry sufficient to impart to at least three  
of the devices three different respective threshold voltages, wherein the  
common masking step comprises masking only portions of some of the  
devices which receive the halo implant; said devices which receive the halo  
implant comprise NMOS field effect transistors; and said portions comprise  
portions of peripheral circuitry devices.

Claim 14: A semiconductor processing method comprising:  
a masking step providing a common mask; and  
an implant step carried out through the common mask, comprising  
conducting a halo implant of devices formed over a substrate comprising  
memory circuitry and peripheral circuitry sufficient to impart to at least three  
of the devices three different respective threshold voltages, wherein the  
common masking step comprises masking only portions of some of the  
devices which receive the halo implant; said devices which receive the halo  
implant comprise PMOS field effect transistors; and said portions comprise  
portions of peripheral circuitry devices.